OSNABRÜCK UNIVERSITY

Embedded Software Systems

A Full-System Perspective on UPMEM Performance

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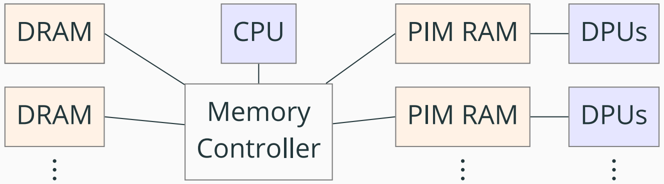
“Processing in Memory” (PIM)



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  - Transparent data processing in DRAM Processing Units (DPUs)
  - No memory controller bottleneck

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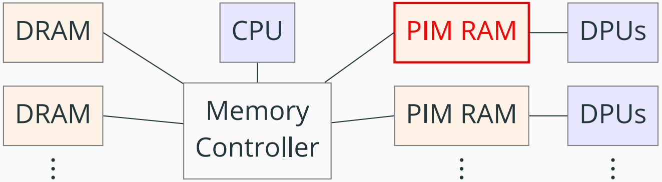

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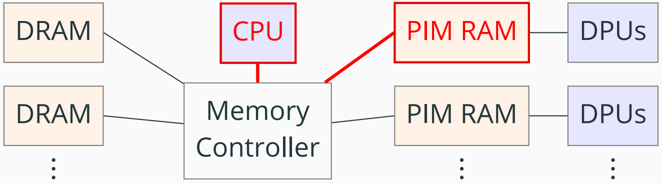

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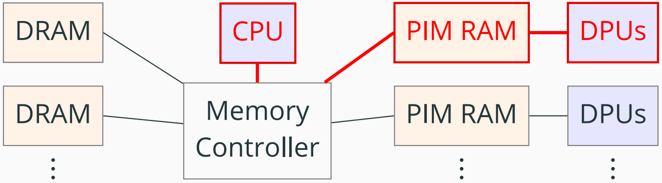

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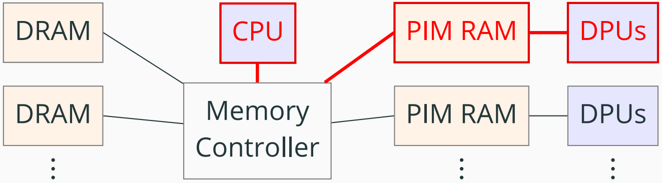

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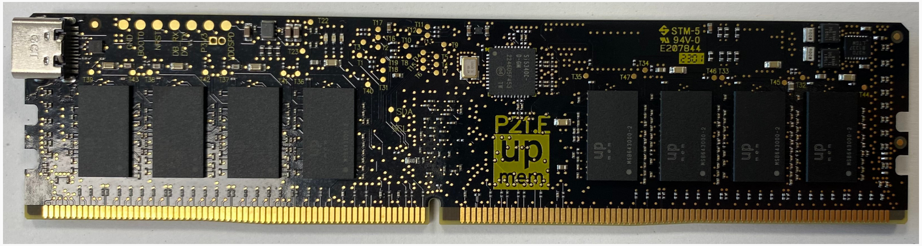
→ How to determine PIM-friendly workloads?

- Research limited to simulators and custom FPGA builds until 2021

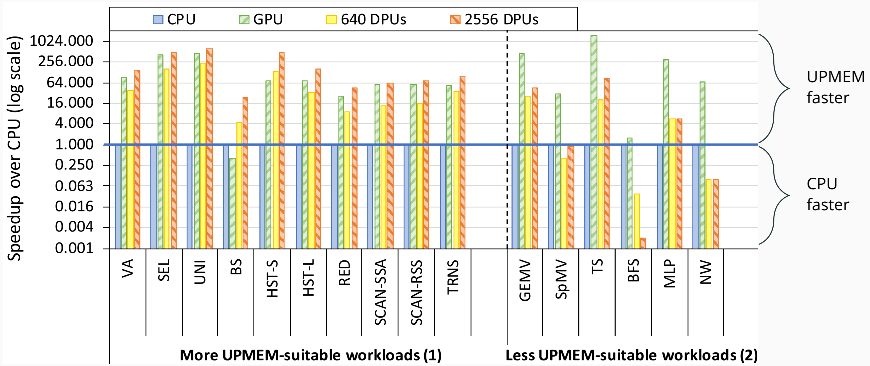
UPMEM PIM



- First (and only) commercially available processing-in-memory platform
  - 8 GB DDR4 modules (2 ranks × 4 GB)
  - 128 DPUs built into memory chips: 32-bit RISC @ 267 . . . 450 MHz
- Popular evaluation target [Góm+22; BJS23]

UPMEM: Promising Results

CPU: 4 threads on Intel Xeon E3-1240



PrIM suite: speedup of UPMEM PIM over quad-core CPU [Góm+22]

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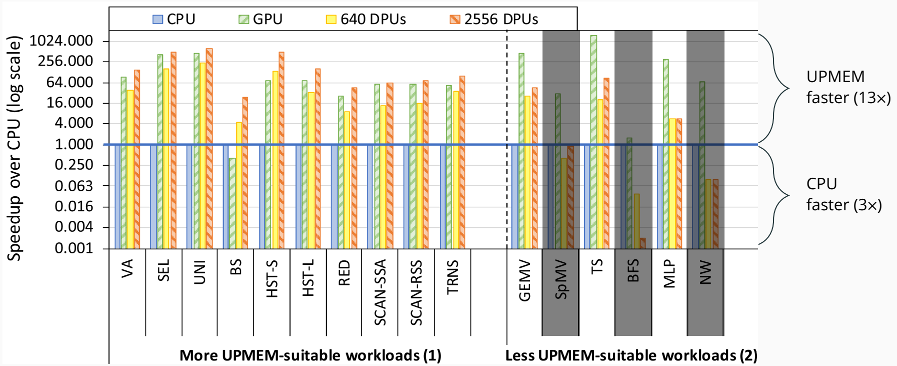
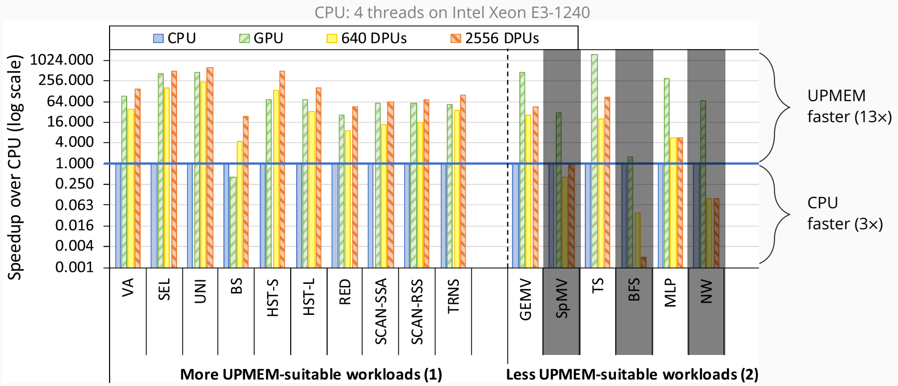


PrIM suite: speedup of UPMEM PIM over quad-core CPU [Góm+22]

⇒ PIM seems useful for DB queries, vector processing, data analysis . . .

UPMEM: Promising Results(?)

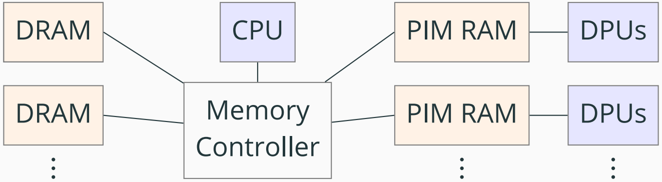


PrIM suite: speedup of UPMEM PIM over quad-core CPU [Góm+22]

. . . when leaving out overhead (assumption: amortized by chained kernels)

Outline

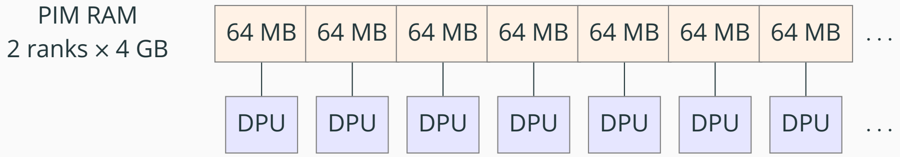
The Ideal PIM Architecture



Common assumption: DPUs behave like additional CPUs [Cor+21]

- No need to port or adjust algorithms
- No need to move data between DRAM and PIM RAM
- DPU execution overhead ≈ CPU scheduling overhead

A Real-World PIM Architecture (UPMEM)



- 64MB chunk of DRAM per DPU, no shared memory
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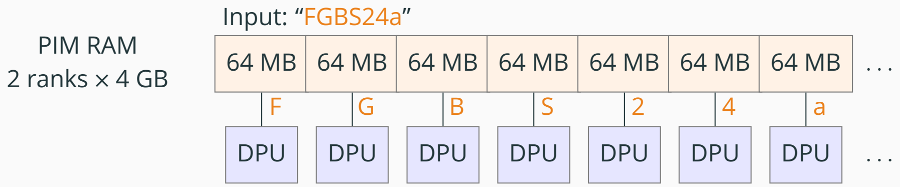

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- Interleaving → PIM RAM ≠ DRAM; SDK mandatory [Dev19]
  → costly data exchange via SDK thread pool on host CPU

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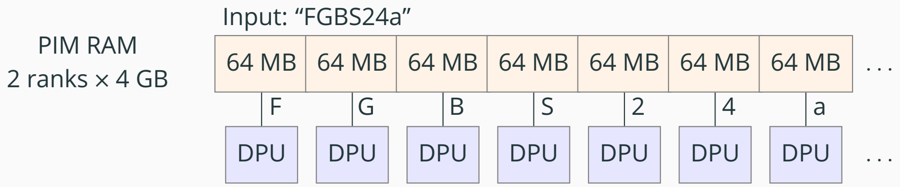

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→ UPMEM PIM ≈ offloading engine; benchmarks must consider this

- Known challenges [Dav95; Lee+10; HB15]; lack of best practices for PIM

Challenges for a Full-System Perspective

- Goal: Identify UPMEM-suitable workloads
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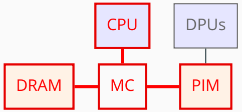

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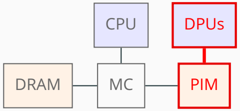

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  - Code and algorithm optimization (different architectures)

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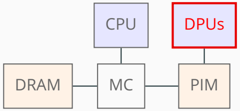

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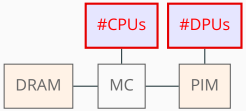

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  - Resource allocation (1 . . . 100s of CPUs vs. 1 . . . 2560 DPUs)

Challenges for a Full-System Perspective

```
make dpus=512 tasklets=16
bin/scan-rss -i 1024
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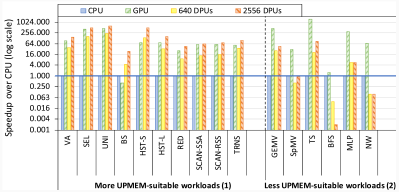
Outline

Foundation: the PrIM Benchmark Suite

- PrIM: comprehensive set of benchmark applications [Góm+22]
- CPU and UPMEM implementations, including
  - Database queries
  - Time series analysis
  - Image, matrix, vector processing



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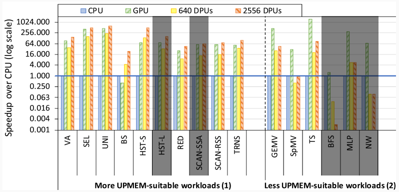
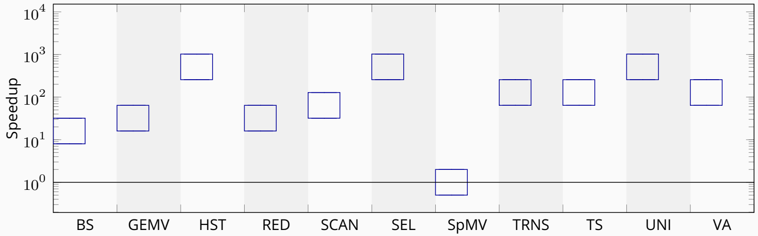


- Source code and data sets (mostly) available
  - Suitable foundation for full-system performance perspective
  - Selection: 8 “UPMEM-suitable” + 3 “less suitable” (but promising) workloads

→ 1st Workshop on Disruptive Memory Systems (DIMES’23) [FLS23]

Reproduction



PIM (kernel only) on 2556 DPUs over four threads on Xeon E3-1240 @ 3.3 GHz (PrIM)

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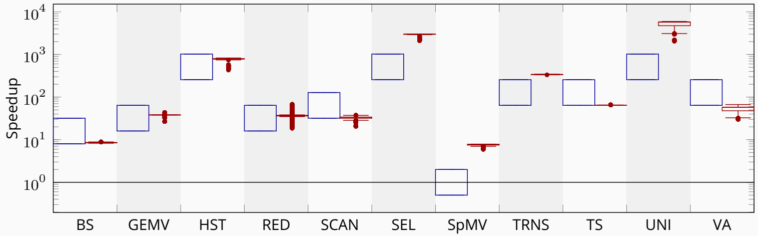

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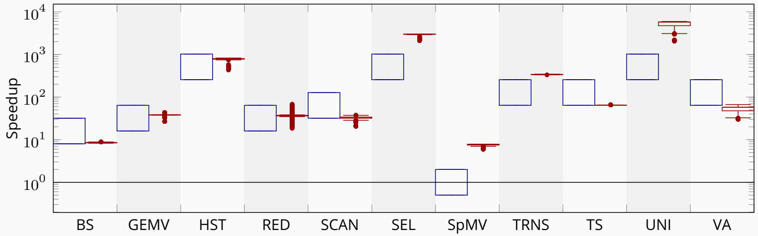

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- 10/11 weak scaling results (1 . . . 64 DPUs, no CPU) reproduced

Reconfiguration Overhead

- UPMEM: allocate set of DPUs and upload application
- Key attribute in FPGA offloading research [Sch+20]
- Not considered in PIM/UPMEM benchmarks

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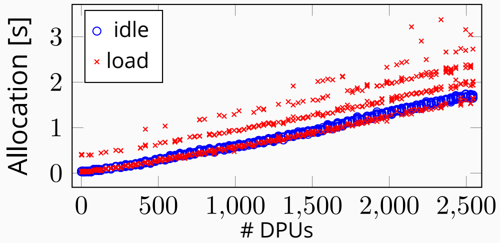

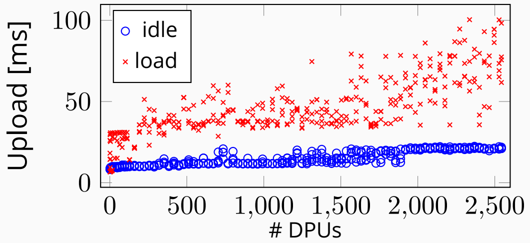

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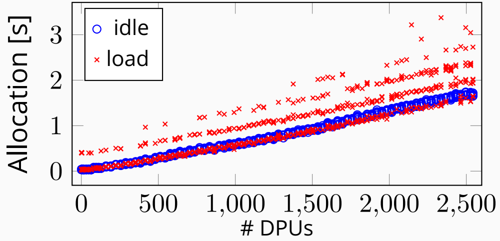
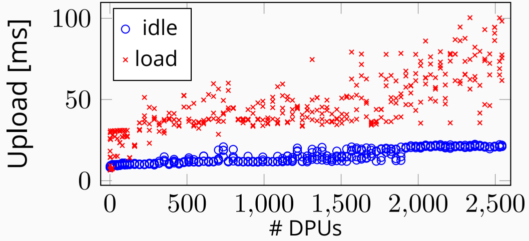
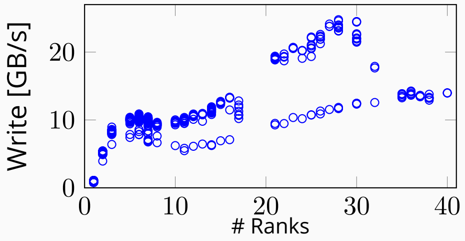


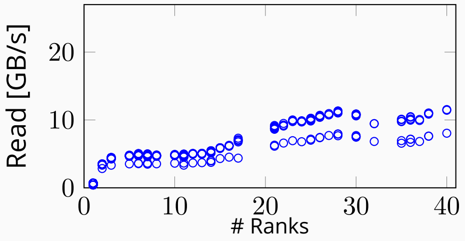


- Allocation can take seconds → short workloads infeasible with current SDK

Data Transfer Overhead

- UPMEM: explicit data transfers via SDK (with internal thread pool)





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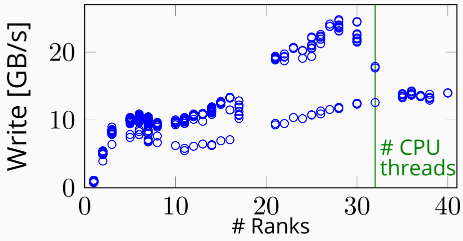

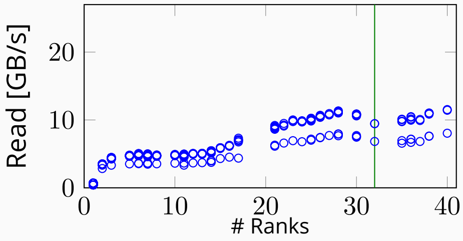

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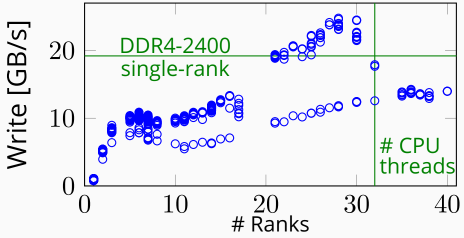

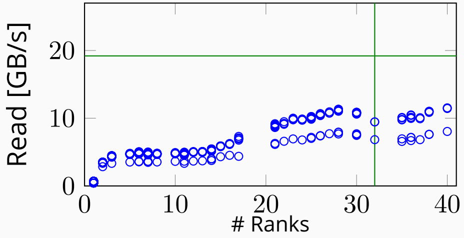

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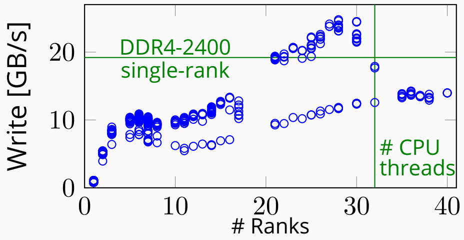
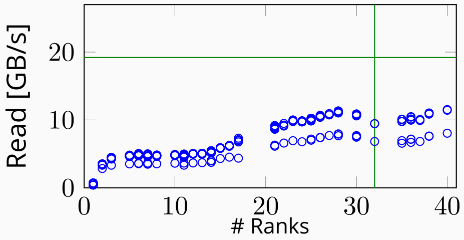


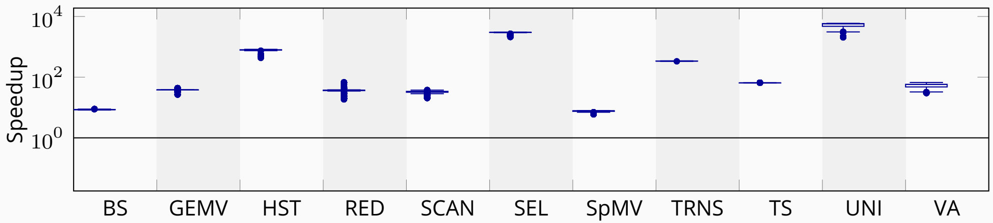


- Base latency in milliseconds range [Góm+22]
  - DRAM → MRAM on UPMEM module (write): 5 . . . 90 ms
  - DRAM ← MRAM on UPMEM module (read): 6 . . . 270 ms

Data Transfer in Benchmarks

- UPMEM mandates DRAM ↔ PIM RAM transfers
- “Amortized overhead”: weak argument (IRAM holds ≤ 4,096 instructions)

$2^{11} + 2^{8}$ = 2304 DPUs vs. 4 threads on Xeon Silver 4215



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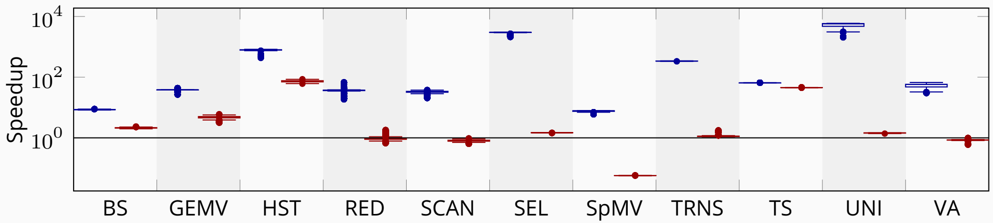

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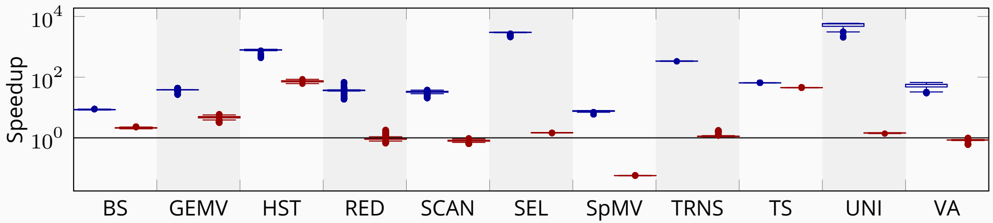

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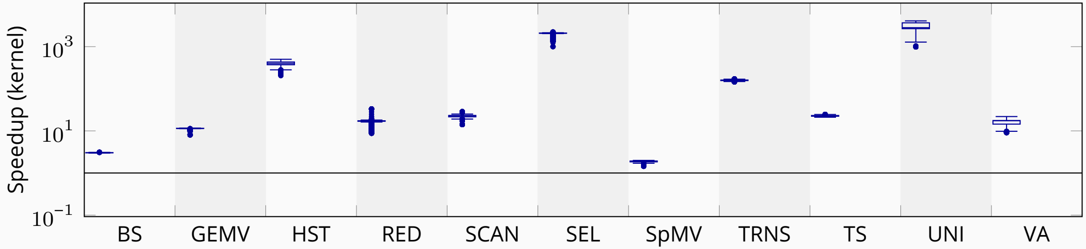
→ Only 7 of 11 workloads still benefit from UPMEM PIM

Resource Allocation

- Speedup benchmarks: how many DPUs vs. how many CPU cores?

$2^{11} + 2^{8}$ = 2304 DPUs vs. Xeon Gold 6152



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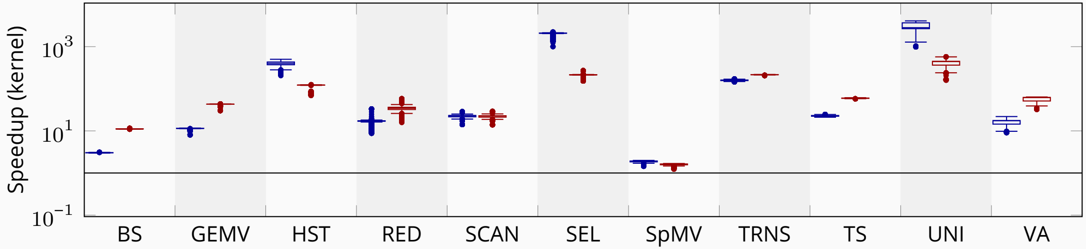

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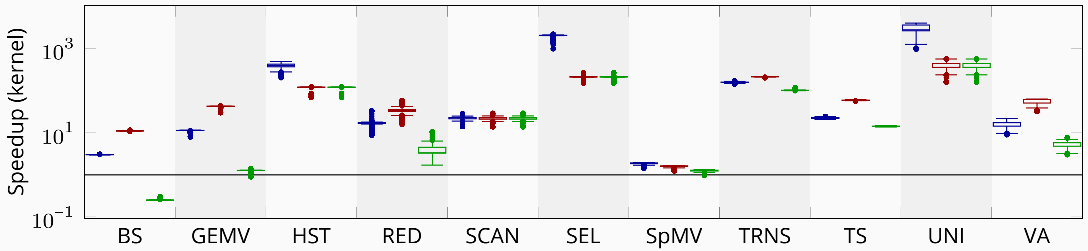

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PIM over best (≤ 88 threads)

(UPMEM cost ≈ 2× CPU-only)

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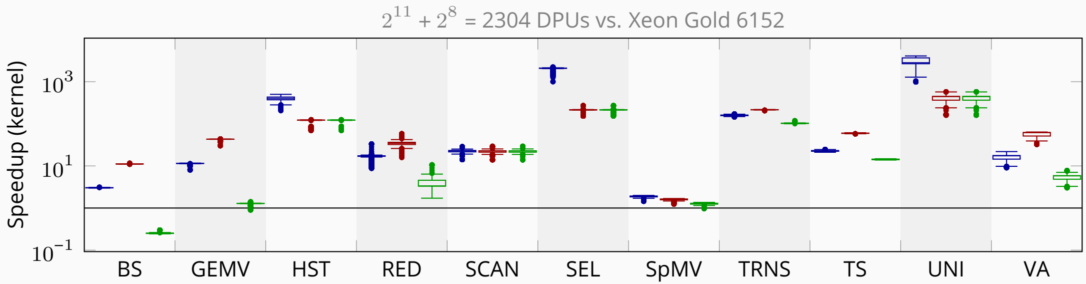

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PIM over best (≤ 88 threads)
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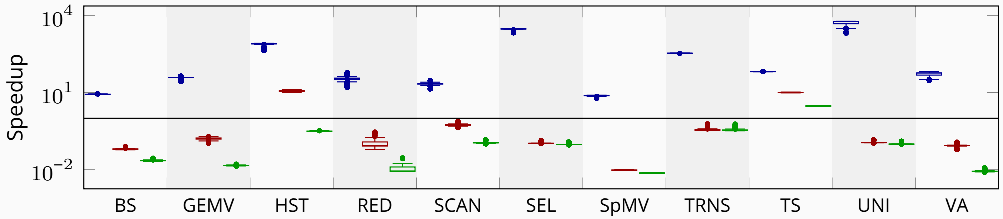
- Variable #DPUs vs. variable #CPUs (parallelization; sub-linear scaling)

Outline

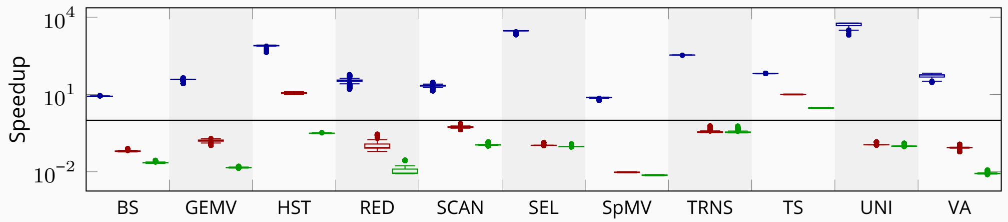
Conclusion



PIM (kernel) / 1 CPU thread PIM (+data) / best CPU PIM (+reconfiguration) / best CPU

- Assumptions matter: only **2 of 11** (**1 of 11**) individual workloads benefit

Conclusion



PIM (kernel) / 1 CPU thread   PIM (+data) / best CPU   PIM (+reconfiguration) / best CPU

- Assumptions matter: only **2 of 11** (**1 of 11**) individual workloads benefit
- Detailed benchmarks are key for evaluating novel technologies: reproducible; overhead-aware; variable resource allocation

References i

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